REMARKS

STATUS OF APPLICATION

Claims 3 and 14 have been canceled. No new claims have been added. Accordingly, claims 1, 2, 4-13, and 15-41 are pending in the present application. Claims 16-41 have been withdrawn from consideration as a result of a restriction requirement. No new matter has been introduced by way of the present amendment.

DRAWINGS

The indication, in the Office Action, that the drawings filed on July 19, 2001 are accepted by the Examiner, is noted with appreciation.

To date, no Notice of Draftsperson's Patent Drawing Review has been received. Applicants respectfully request receipt of this document when it becomes available. Please note that the original drawings filed in the patent application are "formal" drawings.

35 USC § 103 REJECTIONS

Rejection of claims 1-5 over USPAP 2002/0032499 in view of US 6,436,265

The rejection of claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0032499 to Wilson *et al.* (hereinafter referred to as "the Wilson application") in view of U.S. Patent 6,436,265 to Shimada *et al.* (hereinafter referred to as "the Shimada patent"), is respectfully traversed for the reasons set forth hereinafter.

Claim 1, as amended, requires revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of a deposition recipe if a measured thickness of a conductive layer is not within the predetermined tolerance. To establish a *prima facie* case of obviousness, three basic criteria must be met[1]:

> (1) There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, rather than merely in Applicants' disclosure, to modify the reference or to combine reference teachings;
>
> (2) There must be a reasonable expectation for success found in the prior art, rather than in Applicants' disclosure; and
>
> (3) The prior art references must teach or suggest all the claim limitations.

The indication, in the Office Action, that the Wilson application fails to teach revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing, is noted with appreciation. Further, the Shimada patent is silent with regard to revising either a chemical concentration of an electroplating bath or an anode-cathode spacing, as required by claim 1. Accordingly, the Wilson application and the Shimada patent, either singly or in combination, do not teach or suggest all of the limitations of claim 1 and, thus, cannot render the present invention, as set forth in claim 1, obvious.

Further, as both the Wilson application and the Shimada patent are silent with regard to revising either a chemical concentration of an electroplating bath or an anode-cathode spacing, they cannot, either when taken singly or in combination, provide a reasonable expectation of success for controlling a conductive layer deposition process.

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[1] *See* MPEP 2143 and *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Accordingly, the Wilson application and the Shimada patent, either taken singly or in combination, cannot render the present invention, as set forth in claim 1, obvious.

Claim 3 has been canceled. Claims 2, 4, and 5 depend from claim 1. Accordingly, the remarks provided *supra* concerning claim 1 apply equally to claims 2, 4, and 5.

Therefore, it is respectfully requested that the rejection of claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over the Wilson application in view of the Shimada patent, be reconsidered and withdrawn.

Rejection of claims 6-15 over USPAP 2002/0032499 in view of US 6,436,265

The rejection of claims 6-15 under 35 U.S.C. § 103(a) as being unpatentable over the Wilson application in view of the Shimada patent, is respectfully traversed for the reasons set forth hereinafter.

Claim 6, as amended, requires revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least a calculated value representing the measured thickness of a conductive layer, if the calculated value is not within the predetermined tolerance. As discussed *supra* concerning claim 1, neither the Wilson application nor the Shimada patent, either taken singly or in combination, disclose or suggest revising such a parameter. Accordingly, the Wilson application and the Shimada patent, either singly or in combination, cannot render the present invention, as set forth in claim 6, obvious.

Claim 14 has been canceled. Claims 7-13 and 15 depend from claim 6. Accordingly, the remarks provided *supra* concerning claim 6 apply equally to claims 7-14 and 15.

Therefore, it is respectfully requested that the rejection of claims 6-15 under 35 U.S.C. § 103(a) as being unpatentable over the Wilson application in view of the Shimada patent, be reconsidered and withdrawn.

CONCLUSION

Attached hereto is an appendix including a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Wherefore, in view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to contact Daren C. Davis at (817) 578-8616 with any questions, comments or suggestions relating to the referenced patent application.

23720
PATENT TRADEMARK OFFICE

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Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The following is a marked-up version of the changes to the claims that are being made in the attached response to the Office Action dated October 4, 2002.

<u>IN THE CLAIMS</u>:

Claims 3 and 14 have been canceled.

Claims 1 and 6 have been amended as follows, wherein additions are underlined:

1. (Once Amended) A method of controlling a conductive layer deposition process, comprising:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer deposited on the semiconductor wafer;

determining whether the measured thickness of the conductive layer is within a predetermined tolerance; and

revising <u>at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of</u> the deposition recipe if the measured thickness of the conductive layer is not within the predetermined tolerance.

6. (Once Amended) A method of controlling a conductive layer deposition process, comprising:

depositing a conductive layer above a first semiconductor wafer based upon a deposition recipe;

measuring a thickness of the conductive layer at a plurality of locations;

calculating a value representing the measured thickness measured at the plurality of locations;

determining whether the calculated value is within a predetermined tolerance; and

revising at least one parameter selected from the group consisting of a chemical concentration of an electroplating bath and an anode-cathode spacing of the deposition recipe based upon at least the calculated value if the calculated value is not within the predetermined tolerance.

Marked-Up Version

of

Substitute Specification Pages 8 and 9

for

09/909,074

example, silicon dioxide, silicon nitride, silicon oxynitride, or the like, may be formed over the previously formed structures. One or more openings 122 (*e.g.*, vias or trenches) may be then etched through the insulating layer 120.

As illustrated in Figure 2, a barrier metal layer 202 (*e.g.*, titanium nitride, tantalum, tantalum nitride, or the like) may be deposited over the insulating layer 120 to inhibit migration of copper (deposited in a later process step) into silicon structures. A copper seed layer 204 may then be deposited over the barrier metal. Thereafter, a copper layer 206 may be deposited, typically by a electrolytic plating process, over the copper seed layer 204 to fill the openings 122 (Figure 1). This process typically produces the copper layer 206 across the entire wafer. Once a sufficiently thick copper layer 206 has been deposited, the copper layer 206 may be planarized using CMP techniques. In the example illustrated in Figures 1 and 2, the copper layer 206 is applied to the wafer to provide contacts 208 to source/drain regions 110. After planarizing the copper layer 206, further insulating layers (similar to the insulating layer 120) may be applied to the wafer, etched to form additional openings (*e.g.*, trenches and the like), and filled with copper to form electrical interconnections between the previously formed contacts and the like. Thus, the process of applying an insulating layer, etching the insulating layer to form openings, depositing a copper layer thereover, and planarizing the copper layer is repeated as desired to form multilevel metal schemes, such as dual damascene schemes.

It is generally advantageous to optimize the thickness of a copper layer (*e.g.*, the copper layer 206) so that the copper layer 206 is sufficiently thick to properly

conduct electrons as required and is sufficiently thin so that the time and materials required to planarize the copper layer are held to a minimum. Further, it is generally advantageous to optimize the thickness of the copper layer 206 on a wafer-by-wafer basis so that variations in thicknesses of copper layers (*e.g.*, the copper layer 206) on a series of wafers are minimized. Referring now to Figure 3, the illustrated embodiment comprises depositing a conductive layer (*e.g.*, the copper layer 206) on a wafer *J* (block 302), wherein *J* represents a wafer number in a series or lot of wafers. After the conductive layer has been deposited, the thickness of the conductive layer is measured (block 304) and is compared to a predetermined, acceptable thickness tolerance to determine if the thickness of the conductive layer is within acceptable limits (block 306). If the thickness of the conductive layer is not within tolerance, the deposition recipe is revised (block 308) so that the conductive layer on the next wafer (i.e., wafer *J*+1) will have a thickness that is within tolerance. The deposition recipe for an electroplating process controls, for example, the electroplating bath temperature, electroplating chemical concentrations, anode-cathode spacing, the anode power settings, the electroplating deposition time, and the like so that the electroplating process will give the desired thickness of the conductive layer. ~~**[NOTE TO INVENTORS: Please verify the electroplating parameters listed above that can be adjusted and add any other applicable parameters.]**~~ If, however, the thickness of the conductive layer is within tolerance, the next wafer (i.e., wafer *J*+1) is processed (blocks 310, 302) with no changes to the deposition recipe.